I Semester [VLSI Design & Embedded Systems]

USN | | | | | | | | | | |

12EC129

# M.Tech. Degree Examination, Dec.2013/Jan.2014
## SOC Design

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer any FIVE full questions.***



1 a. What is Moore's law? What are the limitations impose by small device geometrics. **(15 Marks)**

b. Compare system-on-based, system-on-chip and system-on-package. **(05 Marks)**

2 a. What is short channel effect? Explain. **(10 Marks)**

b. What is scaling? What are its types? Explain constant voltage scaling. **(10 Marks)**

3 a. Consider an n-channel MOS process with the following parameters : substrate doping density $N_A = 10^{16} cm^{-3}$, polysilicon gate doping density $N_D(gate) = 2 \times 10^{20} cm^{-3}$, gate oxide thickness tox = 50 nm, oxide-interface fixed charge density $N_{OX} = 4 \times 10^{10}$ $cm^{-2}$ and source and drain diffusion doping density $N_D = 10^{17} cm^{-3}$. In addition, the channel region is implanted with p-type impurities (impurity concentration $N_I = 2 \times 10^{11} cm^{-2}$) to adjust the threshold voltage. The junction depth of the source and drain diffusion regions is $x_j = 1.0$ μm. Plot the variation of the zero-bias threshold voltage $V_{TO}$ as a function of the channel length (assume that $V_{DS} = V_{SB} = 0$ and the threshold voltage without the channel implant $V_{TO} = 0.40$ V) **(10 Marks)**

b. Explain : (i) Canonical SOC design (ii) Soft IP versus Hard IP. **(10 Marks)**

4 a. Explain waterfall versus spiral system design flow. **(10 Marks)**

b. Explain system design process. **(10 Marks)**

5 a. What is flash memory? Explain NOR flash memory cell and compare with NAND flash memory cell. **(10 Marks)**

b. What is DRAM? Explain with the design. **(10 Marks)**

6 a. What is network topology? Explain. **(10 Marks)**

b. What are switching strategies? Explain packet switching and its types. **(10 Marks)**

7 a. What are the limitations of traditional ASIC design? **(10 Marks)**

b. Explain extensible processors as an alternative to RTL. **(10 Marks)**

8 a. Explain design of timing closure: logic design issues. **(10 Marks)**

b. What is routing? Explain NOC routing and its schemes. **(10 Marks)**

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